

A

11/09/99
jc625 U.S. PTO
09/436158
SAN FRANCISCO

LAW OFFICES OF
SKJERVEN, MORRILL, MACPHERSON, FRANKLIN & FRIEL LLP
610 NEWPORT CENTER DRIVE, SUITE 330
NEWPORT BEACH, CALIFORNIA 92660
(949) 718-6780

FACSIMILE: (949) 718-6799

November 9, 1999

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Docket No.: M-7744 US

Enclosed herewith for filing is a patent application, as follows:

Inventor: Erasmo Perez and David T. Roman
Title: Semiconductor Package With Exposed Die Pad And Body-Locking Leadframe

jc625 U.S. PTO
09/436158
11/09/99

- X Return Receipt Postcard
- X This Transmittal Letter (in duplicate)
- 12 pages Specification
- 6 pages Claims
- 1 page Abstract
- 3 pages Declaration for Patent Application and Power of Attorney
- 2 pages Assignment
- 1 page Recordation Form Cover Sheet (in duplicate)
- 3 sheets of Drawings

CLAIMS AS FILED fees computer under \$1.9(f)

For	Number Filed		Number Extra	Rate	Basic Fee
Total Claims	20	-20	0	\$ 18.00	\$760.00
Independent Claims	3	-3	0	\$78.00	\$ 0.00

Application contains one or more multiple
dependent claims (total fee)

Fee for Request for Extension of Time

Please make the following charges to Deposit Account 19-2386

- ☒ Total fee for filing the patent application in the amount of \$796.00
- ☒ The Commissioner is hereby authorized to charge any additional fees which
may be required, or credit any overpayment to Deposit Account 19-2386.

EXPRESS MAIL LABEL
NO. EL451052158US

Respectfully submitted,

Don C. Lawrence

Don C. Lawrence
Attorney for Applicants
Reg. No. 31,975

SEMICONDUCTOR PACKAGE WITH EXPOSED DIE PAD AND BODY-LOCKING LEADFRAME

Erasmo Perez
David T. Roman

BACKGROUND

1. Field of the Invention:

This invention relates to packaging of semiconductors in general, and in particular, to a very thin, small outline, thermally enhanced semiconductor package having a coined leadframe that provides a die pad with an exposed surface and features that lock the leadframe more securely to the plastic body of the package.

2. Description of the Related Art:

Integrated circuits ("ICs") are formed on a single die, or "chip," cut from a semiconductor wafer containing a large number of identical dies. The dies are relatively small and fragile, are susceptible to harmful environmental elements, particularly moisture, and generate a relatively large amount of heat in a relatively small volume during operation. Accordingly, ICs must be packaged in affordable, yet robust packages that protect them from the environment, enable them to be reliably mounted to and interconnected with, for example, a printed circuit board ("PCB") populated with associated electronic components, and to effectively dissipate the heat they generate during operation.

Leadframe types of semiconductor packages are well known and widely used in the electronics industry to house, mount, and interconnect a variety of ICs. A conventional leadframe is typically die-stamped from a sheet of flat-stock metal, and includes a plurality of metal leads temporarily held together in a planar arrangement about a central region during package manufacture by a rectangular frame comprising a plurality of expendable “dam-bars.” A mounting pad for a semiconductor die is supported in the central region by “tie-bars” that attach to the frame. The leads extend from a first end integral with the frame to an opposite second end adjacent to, but spaced apart from, the die pad.

During package manufacture, an IC die is attached to the die pad. Wire-bonding pads on the die are then connected to selected ones of the inner ends of the leads by fine, conductive bonding wires to convey power, ground, and signals between the die and the leads.

A protective body of an epoxy resin is molded over the assembly to enclose and seal the die, the inner ends of the leads, and the wire bonds against harmful environmental elements. The rectangular frame and the outer ends of the leads are left exposed outside of the body, and after molding, the frame is cut away from the leads and discarded, and the outer ends of the leads are appropriately formed for interconnection of the package with other, associated componentry.

In a variant of the above configuration, *viz.*, a “land grid array” (“LGA”), or a “leadless chip carrier” (“LCC”) package, the outer portions of the leads are removed

entirely from the package, and a terminal, or "land," is provided on the lower surface of the leads and exposed through the lower surface of the body for mounting and inter-connection of the package to a PCB. In yet another variation, the die pad is "down-set" relative to the plane of the leads such that its lower surface is exposed through the lower surface of the body for enhanced dissipation of heat from the die.

While the foregoing prior art package configurations provide a reasonable compromise between packaging cost and performance, they also include some recognized problem areas where there is a long-felt need for improvement. One of these relates to the problem of making reliable wire bonds to leads that have been made extremely narrow to accommodate an extremely fine lead pitch. In particular, as package sizes decrease, lead densities remain the same or even increase. In response, leads are made much narrower so that they can be placed closer together. At some limiting width and pitch of the leads, the leads become so narrow and close together that it is difficult to make wire bonds to them reliably. It is therefore desirable to provide a leadframe design that can accommodate very narrow, closely pitched leads, yet one in which reliable wire bonds can be made to the leads.

Another problem relates to delamination of the leadframe components from the plastic package body, and the attendant problem of penetration of the package by moisture. In particular, the various parts of a semiconductor package experience greatly different amounts of thermal expansion and contraction with temperature

changes due to the relatively large differences in the coefficients of thermal expansion of their respective materials, e.g., metal, epoxy resin, and silicon.

As a result, the leadframe components can become delaminated from the package body with temperature cycling of the package during manufacture or operation.

5 Where delamination occurs at a boundary of the package body, a microscopic crack is created for the penetration of the package by moisture. This penetration can wreak a two-fold assault on the package: First, the moisture can corrode any metallizations present in its path, resulting in subsequent current leakage through the corrosive path; second, the moisture can expand and contract with temperature cycling of the package,
10 resulting in further propagation of the cracks into the package, and hence, further penetration of the package by moisture. It is therefore desirable to provide a leadframe design that more securely locks the leadframe components to the plastic body of the package, thereby effectively reducing both the amount of delamination of the leadframe from the body and the resulting penetration of the body by moisture.

15

BRIEF SUMMARY OF THE INVENTION

The present invention includes a very thin, small outline, thermally enhanced semiconductor package having a leadframe that provides locking features on a plurality of extremely narrow, closely spaced leads and on an exposed die pad to improve
20 mechanical locking between the leadframe and the plastic body of the package. The improved locking reduces the incidence of delamination between the leadframe and

the package body and increases the resistance of the package to penetration by moisture.

The novel leadframe is made by patterning a metal plate to form: a rectangular frame around a periphery of the plate; a plurality of leads, each having an outer end
5 integral with the frame and an inner end extending toward a central region of the frame; and a die pad disposed in the central region of the frame and adjacent to the inner ends of the leads. The die pad is attached to the frame or to two or more of the leads by two or more tie-bars.

A locking pad is coined into an outer end portion of each lead adjacent to the
10 frame, a bonding pad is coined into an inner end portion of each lead adjacent to the die pad, and a recessed shoulder is coined into the lower surface of the die pad around a central portion thereof. The bonding pads increase the area of the leads adjacent to the die pad to enable reliable bonds to be made to the leads. The locking pads, bonding pads, and recessed shoulder provide locking steps in the leadframe and increase the
15 area of adhesion between the leadframe and an over-molded plastic body to lock the two together more securely and increase their resistance to delamination and the subsequent penetration of the package by moisture. A mounting and interconnection land is defined on the lower surface of each lead between the locking pad on its outer end and the bonding pad on its inner end.

20 A semiconductor package is formed on the leadframe by attaching a semiconductor die to the upper surface of the die pad, wire-bonding the die to selected ones of

the bonding pads, and molding a body of an insulative plastic over the die, the die pad, and the leads such that the locking pads, the bonding pads and the recessed shoulder on the lower surface of the die pad are covered by and interlock with the plastic body. The rectangular frame is exposed at a lateral periphery of the body for its subsequent removal, and the lands and the central portion of the lower surface of the die pad are exposed through a lower surface of the body for their subsequent attachment to a PCB.

A better understanding of the present invention may be had from a consideration of the detailed description below, particularly if such consideration is made in conjunction with the drawings.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Figure 1 is a plan view of a ductile metal plate from which the leadframe of the present invention is etched;

Fig. 2 is a plan view of the leadframe of the present invention resulting from the etching of the plate shown in Fig. 1;

Figs. 3 and 4 are top and bottom plan views, respectively, of the leadframe of the present invention after coining of the leadframe shown in Fig. 2;

Fig. 5 is a top plan view of the leadframe seen in Fig. 3 showing the attachment of a semiconductor die thereto;

Fig. 6 is a cross-sectional, elevation view of the leadframe of the present invention disposed between the inner faces of two coining dies;

Fig. 7 is a cross-sectional, elevation view of one embodiment of a semiconductor package in accordance with the present invention, shown mounted to a PCB; Fig. 8 is a side elevation view of the semiconductor package shown in Fig. 7; and, Fig. 9 is a bottom plan view of the semiconductor package shown in Figs. 7 and 8.

5

DETAILED DESCRIPTION OF THE INVENTION

Figures 1-5 show in plan view the sequential fabrication and partial assembly of one embodiment of the novel leadframe 10 of the present invention. Fabrication of the leadframe begins with the provision of a thin, polygonal plate 12 of a ductile metal (Fig. 1), which is then patterned to form the nascent leadframe 10 (Fig. 2).

In the exemplary square embodiment illustrated in Fig. 1, the plate 12 is about 0.254 millimeters ("mm") thick, about 4 mm on a side, and made of a copper alloy. Other metals suitable for use in the leadframe 10 include aluminum and iron-nickel (Kovar) alloys.

Figure 2 is a top plan view of the leadframe 10 patterned from the plate 12 shown in Fig. 1. The leadframe 10 comprises a rectangular frame 14 defined around a periphery of the plate 12; a plurality of leads 16, each having an outer end portion 18 integral with the frame 14 and an inner end portion 20 extending toward a central region of the frame, the center of which is marked by a cross; and, a die pad 22 disposed in the central region of the frame and adjacent to the inner ends of the leads. In the

embodiment illustrated, the die pad 22 is attached directly to the frame 14 by two or more tie-bars 24, or indirectly through two or more of the leads 16, as shown in Fig. 2.

In the exemplary embodiment illustrated in Fig. 2, the leads 16 are about 0.178 mm wide, about 0.254 mm long, and spaced at a pitch of about 0.500 mm. The die pad 22 is about 2.120 mm on a side. The leadframe 10 can be patterned from the plate 12 by, e.g., die-stamping, etching, using photolithography techniques, electrical discharge machining ("EDM"), or by laser-beam cutting.

Those of skill in the art will recognize the difficulty of making reliable wire bonds to the very narrow, closely pitched leads 16. To overcome this problem, and to provide features on the leadframe 10 for more effectively locking the leadframe to a plastic package body 66 (shown as broken outline in Figs. 2-5) molded over it, the leadframe is subjected to a coining process, which is illustrated in an enlarged cross-sectional view in Fig. 6.

As shown in Fig. 6, after patterning, the planar leadframe 10 is placed between the opposing faces of an upper coining die 26 and a lower coining die 28. The upper face 30 of the lower die 28 includes three raised surfaces 32, 34, 36 that, in a plan view (not illustrated) comprise three concentric rectangles. The opposing lower face 38 of the upper die 26 is substantially flat.

Since the metal of the leadframe 10 is substantially incompressible, the effect of the local coining forces exerted by the dies on a given volume of the metal is to

displace the metal laterally wherever such flow is unrestricted, i.e., its thickness is decreased, its length and/or width is increased, while its volume remains the same.

Thus, when the two dies 26, 28 are brought together forcefully in the direction of the arrows shown, the raised surface 32 coins a locking pad 40 into the outer end portion 18 of each lead 16 adjacent to the frame 14; the raised surface 34 coins a bonding pad 42 into the inner end portion 20 of each lead 14 adjacent to the die pad 22; and, the raised surface 36 coins a recessed shoulder 44 into the lower surface of the die pad 22 around a central portion 46 thereof. A mounting and interconnection land 48 is also defined on the lower surface of each lead 16 between the locking pad 40 on its outer end 18 and the bonding pad 42 on its inner end 20.

Figures 3 and 4 are top and bottom plan views, respectively, of the leadframe 10 after coining, and show the spatulate locking pads 40 and bonding pads 42 on the opposite ends of the respective leads 16, and the recessed shoulder 44 on the die pad 22, resulting from the coining process. An enlarged cross-sectional view of the coined leadframe 10 is shown in Fig. 7.

It will be noted that the upper surface of the leadframe 10 remains substantially planar after coining, whereas, the lower surface of the leadframe comprises a plurality of stepped, or recessed, plateaus where coining has taken place, as shown by the cross-hatched areas in Fig. 4. In the particular embodiment illustrated in the figures, the lower surfaces 50 of the locking pads 40 are coined to a depth of about 0.076 mm, the lower surfaces 52 of the bonding pads 42 are coined to a depth of about 0.127 mm, and

the lower surface 54 of the recessed shoulder 44 is coined to a depth of about 0.051 mm.

The plurality of steps created in the leads 16 and the die pad 22 by these recessed surfaces, combined with the increased adhesion area of the surfaces defining them, act as "keys" to more effectively lock the leadframe 10 into a surrounding body of plastic and thereby resist delamination between the two. This increased adhesion also increases the resistance of the package to the propagation of cracks from an exterior boundary of the package, and hence, a subsequent penetration of the package by moisture. Additionally, the bonding pads 42 effectively enlarge the inner end portions 20 of the leads 16 immediately adjacent to the die pad 22 so that reliable wire bonds can easily be made to the otherwise extremely narrow leads.

Figure 5 illustrates the attachment of a semiconductor die 56 to the upper surface of the die pad 22. The die 56 may be attached with a layer of an adhesive 58 (see Fig. 7), a layer of a double-backed adhesive tape, or by soldering it to the die pad. The die 56 is electrically connected to the leads 16 by a plurality of conductive wires 60 bonded at opposite ends to contact pads 62 on a top surface of the die and selected ones of the bonding pads 42 on the leads, respectively (see Fig. 5). The wire bonding can be effected using either ultrasonic or thermo-compression bonding techniques. It may be noted that the bonding pads 42 on the leads 16 connected to the tie-bars 24 make ample provision for the "down-bonding" of grounding wires 64 from the die 56 to the die pad 22.

After the die 56 has been attached to the die pad 22 and wire bonded to the leads 16, the leadframe 10 is placed in the cavity of a clam-shell mold (not illustrated), and a molten, insulative plastic, e.g., an epoxy resin, is injected into the cavity to form a protective body 66 over the die, the die pad, and the leads to seal and protect them

5 from the environment. The plastic body 66 of the resulting semiconductor package 68 completely envelopes the leadframe 10 such that it surrounds the locking pads 40, the bonding pads 42, and the recessed shoulder 44 on the lower surface of the die pad and interlocks with them to resist delamination between the body and the leadframe. The rectangular frame 14 (shown dotted in Fig. 7) of the leadframe 10 is exposed outside

10 of the lateral periphery of the body 66, and is subsequently cut away from the body and discarded in a finishing operation to leave the outer ends 70 of the locking pads 40 exposed through the side surfaces 72 of the package 68 (see Fig. 8). The central portion 46 of the lower surface of the die pad 22 and the rectangular lands 48 on the lower surfaces of the leads 16 are exposed through the lower surface 74 of the body 66 (see Fig.

15 9) for their subsequent attachment to a PCB 76, as illustrated in the cross-sectional view of Fig. 7. The mounting and interconnection lands 48 and the exposed central portion 46 of the die pad 22 can be attached and electrically connected to the PCB by a solder joint, or, in a low-temperature attachment, by a layer 78 of a filled, electrically and thermally conductive adhesive.

The thin, small outline, LGA semiconductor package 68 incorporating the coined leadframe 10 of the invention and shown in Figs. 7-9 is about 4 mm on a side , and about 1 mm thick.

Those skilled in the packaging art will understand that many variations of the particular embodiments of the novel leadframe and package illustrated and described
5 herein are possible, depending on the particular problem at hand. For example, although a square package 68 is illustrated in the figures, a rectangular or polygonal package is easily confectioned in accordance with teachings herein. Similarly, fewer or greater numbers of leads 16 can be incorporated into the package, on either two, or all
10 sides thereof. Further, the leads 16 can be extended outside of the body 66 of the package 68 and the lands 48 over-molded with plastic to yield a package with peripheral leads, such as those found in a conventional "quad-flat" package.

Accordingly, the particular embodiments illustrated and described herein should be understood as exemplary in nature only, and not as limitations on the scope
15 of the invention, which is defined instead by that of the claims appended hereafter.

WHAT IS CLAIMED IS:

1. A method for making a leadframe for a semiconductor package, comprising:

5 providing a polygonal plate of metal having an upper surface, an opposite, lower surface, and a thickness between the upper and lower surfaces;

10 patterning the plate to form a leadframe therefrom, the leadframe including a polygonal frame around a periphery thereof, a plurality of leads, each having an outer end integral with the frame and an inner end extending toward a central region of the frame, and a die pad attached to the frame in the central region thereof and adjacent to the inner ends of the leads, the leads and the die pad each having upper and lower surfaces coplanar with the upper and lower surfaces of the plate, respectively;

forming a spatulate locking pad into an outer end portion of each lead adjacent to the frame; and,

15 forming a spatulate bonding pad into an inner end portion of each lead adjacent to the die pad, the locking pad and the bonding pad on each lead defining between them a land on the lower surface of the lead.

2. The method of claim 1, wherein the leadframe is patterned from the plate
20 by die-stamping, etching, electrical discharge machining, or laser-beam cutting.

3. The method of claim 1, further comprising forming a recessed shoulder into the lower surface of the die pad around a central portion thereof.

4. The method of claim 3, wherein the locking pad and the bonding pad on each lead are formed into the lead from the lower surface thereof.

5. The method of claim 4, wherein the locking pads, the bonding pads, and the recessed shoulder are formed by coining.

6. The method of claim 5, wherein the locking pads, the bonding pads, and the recessed shoulder are respectively coined to different depths.

7. The method of claim 5, wherein the bonding pads are coined to a depth of about half the thickness of the plate.

15

8. A method for making a semiconductor package, comprising:
patterning a polygonal metal plate to form a leadframe therefrom, the leadframe including a polygonal frame around a periphery thereof, a plurality of leads, each having an outer end integral with the frame and an inner end extending toward a central region thereof, and a die pad attached to the frame in the central region thereof

and adjacent to the inner ends of the leads, the frame, the leads and the die pad each having coplanar upper and lower surfaces, respectively;

forming a spatulate locking pad into an outer end portion of each lead adjacent to the frame, a spatulate bonding pad into an inner end portion of each lead adjacent to the die pad, and a recessed shoulder into the lower surface of the die pad around a central portion thereof, the locking pad and the bonding pad on each lead defining between them a land on the lower surface of the lead;

attaching a semiconductor die to the upper surface of the die pad;

electrically connecting the die to selected ones of the bonding pads; and,

molding a body of an insulative plastic over the die, the die pad, and the leads such that the plastic body surrounds the locking pads, the bonding pads and the recessed shoulder on the lower surface of the die pad and interlocks with them, and such that the rectangular frame is exposed at a lateral periphery of the body, and the lands and the central portion of the lower surface of the die pad are exposed at a lower surface of the body.

9. The method of claim 8, further comprising severing the leads at the lateral periphery of the body and removing the rectangular frame from the package.

10. The method of claim 8, wherein the locking pads, the bonding pads and the recessed shoulder are coined into a lower surface of the leadframe.

11. The method of claim 8, wherein electrically connecting the die to selected ones of the bonding pads comprises wire-bonding pads on an upper surface of the die to the bonding pads on the leads.

5

12. The method of claim 8, wherein the pads on the die are wire-bonded to the bonding pads on the leads by an ultrasonic or a thermo-compression bonding method.

13. A semiconductor package, comprising:

10 a metal leadframe, including a plurality of leads arrayed around a central region thereof, each lead having an outer end extending away from the central region and an inner end extending toward the central region;

a locking pad in an outer portion of each lead adjacent to its outer end;

a bonding pad in an inner portion of each lead adjacent to its inner end;

15 a land defined on a lower surface of each lead between the locking pad and the bonding pad; and,

a die pad attached to the leadframe in the central region thereof and adjacent to the inner ends of the leads, the die pad having an upper surface and a lower surface, the lower surface having a central portion and a recessed shoulder extending around
20 the central portion.

14. The semiconductor package of claim 13, wherein the die pad is attached to the frame or to at least one of the leads by at least one tie-bar.

15. The semiconductor package of claim 13, wherein each of the leads is about 0.18 mm wide, and wherein the leads have a pitch of about 0.5 mm.

16. The semiconductor package of claim 15, wherein each of the bonding pads is about 0.254 mm wide.

17. The semiconductor package of claim 13, wherein the lands are rectangular.

18. The semiconductor package of claim 13, further comprising:

a semiconductor die attached to the upper surface of the die pad;

a plurality of conductive wires bonded at opposite ends to pads on a top surface

of the die and selected ones of the bonding pads on the leads, respectively; and,

a body of an insulative plastic molded over the die, the die pad, and the leads

such that the plastic body surrounds the locking pads, the bonding pads and the re-

cessed shoulder on the lower surface of the die pad and interlocks with them, and such

that the lands and the central portion of the lower surface of the die pad are exposed

through a lower surface thereof.

19. The semiconductor package of claim 13, wherein the leadframe comprises an alloy of copper, aluminum, or iron and nickel.

20. The semiconductor package of claim 18, wherein the insulative plastic of
5 the body comprises an epoxy resin.

20150417023

SEMICONDUCTOR PACKAGE WITH EXPOSED DIE PAD AND BODY-LOCKING LEADFRAME

Erasmo Perez
David T. Roman

5

ABSTRACT OF THE DISCLOSURE

A very thin, small outline, thermally enhanced semiconductor package includes
10 a leadframe that is coined to form locking features on an exposed die pad and on a plu-
rality of extremely narrow, closely spaced leads. The coined features improve the me-
chanical locking between the leadframe and the plastic body of the package to increase
their resistance to delamination and subsequent penetration by moisture, and enable
reliable wire bonds to be made to the otherwise extremely narrow leads.

15

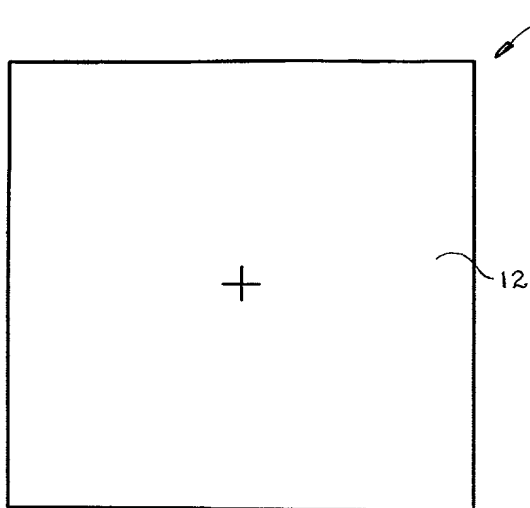


Fig. 1

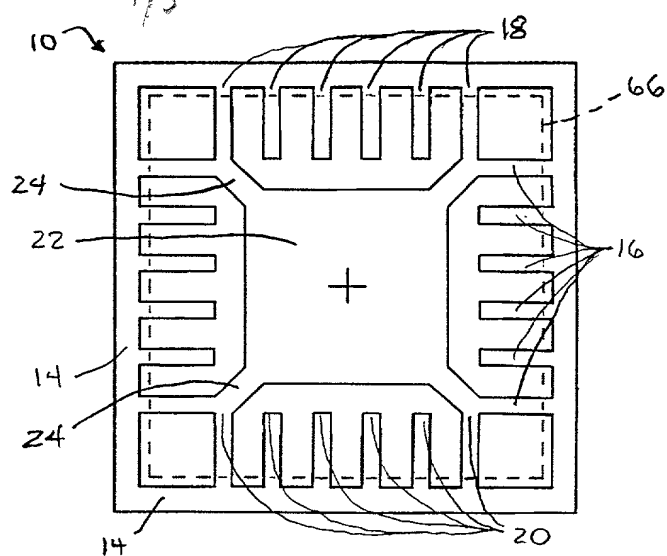


Fig. 2

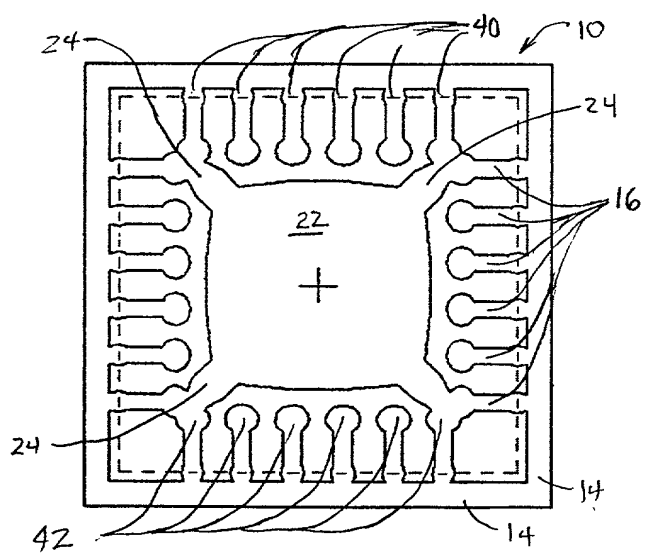


Fig. 3

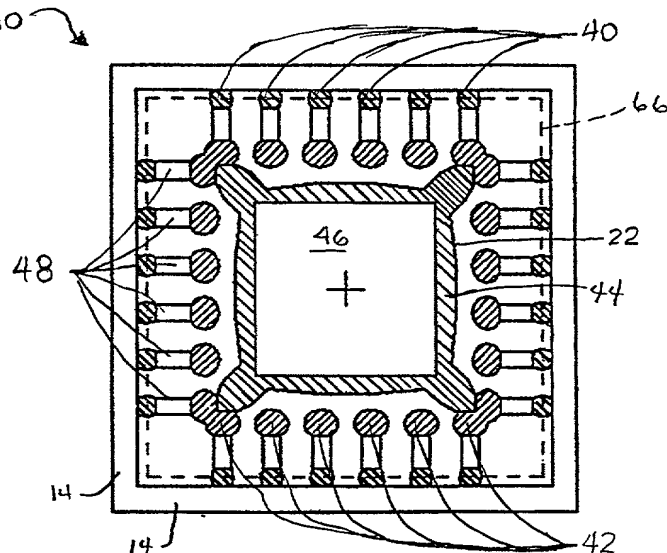


Fig. 4

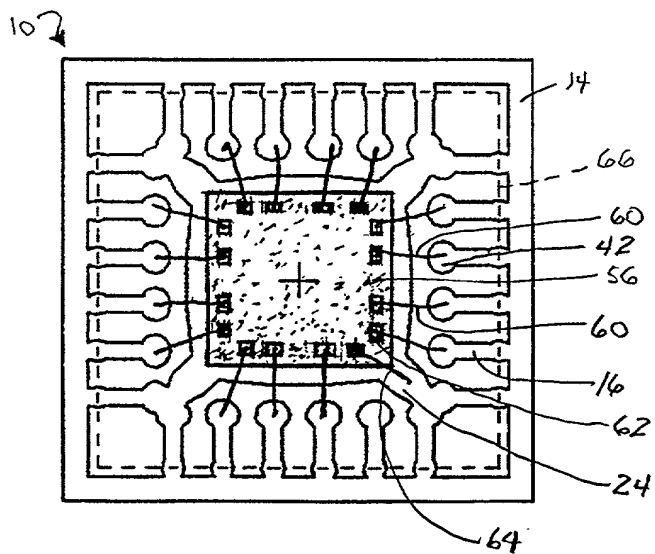
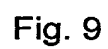
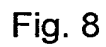
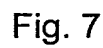


Fig. 5

2007-04-05 1/3

[illegible]

[illegible]

DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am an original, first and joint inventor of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

MLP Deep Coining Option

which (check) ☒ is attached hereto.
☐ and is amended by the Preliminary Amendment attached hereto.
☐ was filed on _____ as Application Serial No.
☐ and was amended on ____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A			<input type="checkbox"/>	<input type="checkbox"/>

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

Alan H. MacPherson (24,423); Brian D. Ogonowsky (31,988); David W. Heid (25,875); Norman R. Klivans (33,003); Edward C. Kwok (33,938); David E. Steuber (25,557); Michael Shenker (34,250); Stephen A. Terrile (32,946); Peter H. Kang (40,350); Ronald J. Meetin (29,089); Ken John Koestner (33,004); Omkar K. Suryadevara (36,320); David T. Millers (37,396); Kent B. Chambers (38,839); Michael P. Adams (34,763); Robert B. Morrill (43,817); Michael J. Halbert (40,633); Gary J. Edwards (41,008); William B. Tiffany (41,347); James E. Parsons (34,691); Daniel P. Stewart (41,332); Philip W. Woo (39,880); John T. Winburn (26,822); Tom Chen (42,406); Fabio E. Marino (43,339); William W. Holloway (26,182); Don C. Lawrence (31,975); Marc R. Ascolese (42,268); Carmen C. Cook (42,433); David G. Dolezal (41,711); Roberta P. Saxon (43,087); Bernice Chen (42,403); Mary Jo Bertani (42,321); Dale R. Cook (42,434); Sam G. Campbell (42,381); Matthew J. Brigham (44,047); Hugh H. Matsubayashi (43,779); Margaret M. Kelton (44,182); Joseph T. VanLeeuwen (44,383); Patrick D. Benedicto (40,909); T.J. Singh (39,535); Shireen Irani Bacon (40,494); Rory G. Bens (44,028); George Wolken, Jr. (30,441); John A. Odozynski (28,769); and Cameron K. Kerrigan (44,826).

Please address all correspondence and telephone calls to:

Don C. Lawrence
Attorney for Applicant(s)
SKJERVEN, MORRILL, MacPHERSON, FRANKLIN & FRIEL LLP
25 Metro Drive, Suite 700
San Jose, California 95110-1349

Telephone: 949-718-6780
Facsimile: 949-718-6799

I declare that all statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties including fine or imprisonment or both as set forth under 18 U.S.C. 1001, and that violations of this paragraph may jeopardize the validity of the application or this document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom.

